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ABSTRACT OF THE DISCLOSURE

A method of controlling a synchronous memory device comprising issuing a write request to the memory device, wherein in response to the write request, the memory device samples first and second portions of data. The first portion of data is provided to the memory device synchronously with respect to a rising edge transition of an external clock signal. A second portion of data is provided to the memory device synchronously with respect to a falling edge transition of the external clock signal. A memory controller for controlling a synchronous memory device comprises output driver circuitry to output data. The output driver circuitry outputs a first portion of data in response to a rising edge transition of the first external clock signal. In addition, the output driver circuitry outputs a second portion of data in response to a falling edge transition of the first external clock signal.